

# Ultra-Low-Noise Millimeter-Wave Pseudomorphic HEMT's

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**Abstract**—Pseudomorphic HEMT's (termed PHEMT's) with gate lengths of one tenth micrometer based on the AlGaAs/InGaAs/GaAs material system have achieved very low noise millimeter-wave performance. The room-temperature device noise figure at 43 GHz is measured to be 1.32 dB (noise temperature = 103 K) with 6.7 dB of associated gain; when cooled to 17 K physical temperature, the noise figure falls to 0.36 dB (noise temperature = 25 K) with 6.9 dB of associated gain. These pseudomorphic devices also show improved sensitivity to input noise match ( $N = 0.13$  at 43 GHz) compared with conventional HEMT's and MESFET's. These pseudomorphic HEMT devices have the lowest noise temperature (N.F.) and noise sensitivity (normalized to frequency) of any GaAs device yet reported.

## I. INTRODUCTION

**B**OTH PRESENT and future microwave and millimeter-wave systems will directly benefit from the improved performance offered by high electron mobility transistors (HEMT's). In contemporary high-performance receivers, where the *noise figure* is the paramount figure of merit, HEMT's have replaced MESFET's to reduce noise, improve gain, and reduce noise match sensitivity. The high cutoff frequency ( $f_T$ ) offered by HEMT's is also valuable in manufacturing both wide-band and high-gain amplifiers. Commercially available HEMT's (for example [1]–[4]) are widely used to achieve high-performance multistage amplifiers.

There is a strong shift toward higher frequencies ( $Ka$ -band through millimeter waves) in systems applications in the areas of satellite communications, remote sensing, missile radar, broad-band EW receivers, and radio astronomy. Here devices which possess performance superior to that of currently available AlGaAs/GaAs HEMT's are required. The pseudomorphic GaInAs on GaAs HEMT's as reported herein and in [5] and [6] are shown to be excellent low-noise amplifier elements. The pseudomorphic HEMT's (PHEMT's) offer the ability to improve receiver signal-to-noise ratio by acting as a low-noise gain element in front of mixers and other lossy elements. Significant gain has been demonstrated by pseudomorphic HEMT's at millime-

ter-wave frequencies (11.2 dB at 96 GHz) with gain extending to an  $f_{\max}$  of 350 GHz [7]. It is anticipated that HEMT's based upon pseudomorphic AlGaAs/InGaAs/GaAs and AlInAs/GaInAs/InP will rapidly extend the use of three-terminal devices to systems operating at well over 100 GHz.

One key to pseudomorphic HEMT gain and noise performance is the superior electron transport properties of this material structure. The InGaAs pseudomorphic channel provides enhanced mobility (1.3 times greater) and electron velocity (1.5 times greater) compared to conventional GaAs channel HEMT's. The sheet carrier charge densities in the InGaAs channel are twice those in the GaAs HEMT channel because of the larger conduction band discontinuity that exists at the AlGaAs/InGaAs heterojunction interface as compared to the AlGaAs/GaAs heterojunction. PHEMT's also show improved carrier confinement and reduced "short-channel effects" compared to conventional HEMT's because the quantum-well channel structure confines charge on both sides of the channel by heterojunction barriers.

PHEMT's employ lower concentrations of aluminum in the AlGaAs donor layer than conventional HEMT's. Hence PHEMT's eliminate certain problems associated with high Al concentrations in regular HEMT's, such as excessive trapping, low-temperature  $I$ – $V$  collapse, persistent photoconductivity, and the need for illumination to achieve a good noise figure at low temperature.

In order to fully exploit the benefits of the pseudomorphic materials, extremely short gate length devices with low parasitic resistances and capacitances are required. Advanced processing procedures such as E-beam lithography, air-bridge interconnects, and low-resistance ohmic contacts have been developed to yield pseudomorphic devices with an ultralow noise figure and good gain up through millimeter-wave frequencies.

## II. DEVICE DESCRIPTION

A schematic cross section of the PHEMT is shown in Fig. 1. The layers are grown by molecular beam epitaxy on high-purity 3-in-diameter LEC GaAs substrates. The layer structure is composed of a highly doped  $n^+$  GaAs contact layer, a transition layer of AlGaAs where both the aluminum composition and the silicon doping are graded, a

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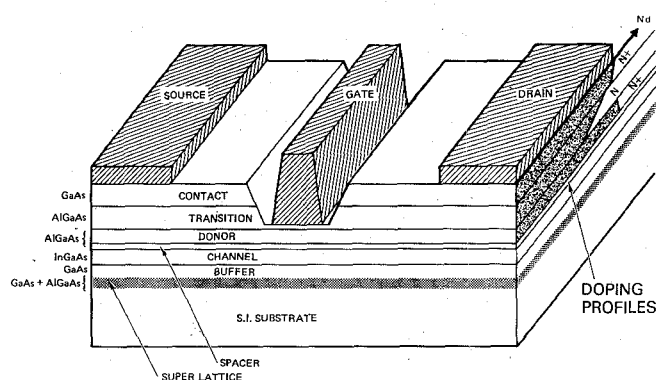


Fig. 1. Pseudomorphic HEMT cross section showing physical layout, layer structure, and doping profiles.

uniformly doped AlGaAs donor layer, a thin undoped AlGaAs spacer layer, an undoped InGaAs high mobility channel layer, an undoped GaAs layer, and an undoped GaAs/AlGaAs superlattice buffer.

The highly doped gallium arsenide contact layer yields a low-resistance ( $R_c = 0.09 \Omega \cdot \text{mm}$ ) ohmic contact to the semiconductor sandwich and acts as a cap to prevent the underlying aluminum gallium arsenide from oxidizing. The transition layer serves to enhance the contact to the 2-D electron gas and establishes the Schottky barrier gate on lightly doped semiconductor material, thus improving breakdown and gate leakage. The AlGaAs donor layer supplies the free carriers to the channel while the spacer improves transport in the channel by reducing Coulomb scattering. The pseudomorphic channel is designed and grown to yield good transport properties and acceptable lattice mismatch strain. Hall test samples exhibit mobility of  $6250 \text{ cm}^2/\text{V} \cdot \text{s}$  at 300 K and  $24900 \text{ cm}^2/\text{V} \cdot \text{s}$  at 77 K. The GaAs (buffer) layer acts as a back-side heterojunction to aid carrier confinement into the channel and reduces charge injection into the buffer. The superlattice structure further confines carriers to the channel region and acts as a barrier to impurity diffusion from the semi-insulating substrate during MBE growth.

Wafer processing is accomplished using a "mix-and-match" lithography approach. E-beam direct write is employed for the gate and gate feed patterns while photolithography is used for all other device layers. This processing strategy achieves significantly higher throughput than an all E-beam fabrication approach. E-beam pattern edge acuity, layer-to-layer realignment accuracy, and resist profile control are commensurate with achieving high-yield PHEMT's with gate lengths that are one tenth micrometer.

The PHEMT devices employ mesa isolation. AuGeNi in combination with rapid thermal alloying is used to form the source-drain ohmic contacts. Gates that are one tenth micrometer are aligned to optically defined ohmic contact patterns and are exposed using a Cambridge EBMF 10.5 E-beam lithography system. Gate exposures are done at a beam voltage of 40 keV, a beam current of 1 nA, and a field size of 1.6 mm by 1.6 mm. Spray development using a

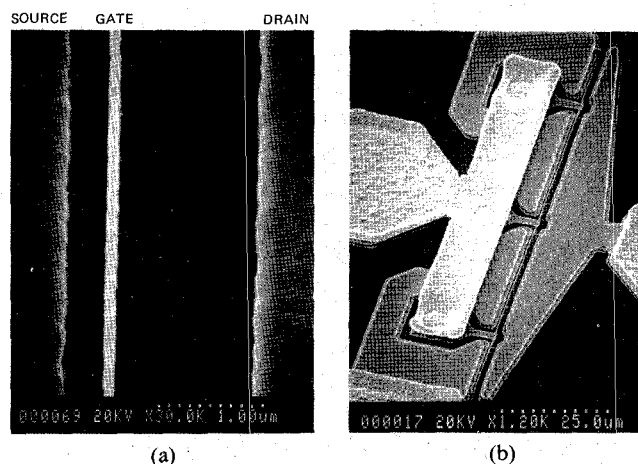


Fig. 2. SEM micrograph of  $100 \mu\text{m} \times 0.1 \mu\text{m}$  PHEMT. (a) Close-up of channel region. (b) Overview of device.

wafer track produces a uniform resist opening of one tenth micrometer with an undercut profile necessary for high-yield lift-off gate metal formation. A highly controlled chemical etch technique is employed to remove the  $\text{n}^+$  GaAs contact layer locating the Schottky-barrier gate electrode in a recess a uniform distance from the InGaAs channel. The gate-to-channel spacing is critical because it directly affects the device transconductance and capacitance. The recess etch employed produces very little E-beam resist undercut so that the deposited gate metal is positioned a short distance from the edge of the  $\text{n}^+$  source contact (see Fig. 1). The lateral separation between the gate and the edge of the  $\text{n}^+$  GaAs contact influences the source and drain resistances, output conductance, and the source-to-drain feedback capacitance. PHEMT noise and gain performance is directly related to the position of the gate in the recess and the recess width [7].

The gate metal employed is Ti/Pt/Au (deposited by E-gun evaporation) and is nominally trapezoidal in cross section after lift-off [8]. Fig. 2(a) shows an SEM photograph of the gate that is one tenth micrometer in length and its relative placement with respect to the source/drain ohmic contacts. The gate is intentionally offset to within  $0.35 \mu\text{m}$  of the source metal contact to reduce parasitic resistance. The edge of the gate recess extends about  $0.07 \mu\text{m}$  on either side of the gate electrode.

Air bridges form the low-capacitance and low-resistance interconnects to the gate feeds. The air bridges and bond pads are electroplated gold to a thickness of  $1.25 \mu\text{m}$  to reduce resistance and facilitate bonding. An overview of the PHEMT is shown in Fig. 2(b). The total active gate periphery is  $100 \mu\text{m}$  and the three gate feeds provide the equivalent resistance of six gates connected in parallel.

### III. DC, MICROWAVE, AND MILLIMETER-WAVE PERFORMANCE

Typical dc source/drain current and transconductance versus gate voltage curves for a  $100 \mu\text{m} \times 0.1 \mu\text{m}$  pseudomorphic HEMT are shown in Fig. 3. The measurements are carried out at  $V_{ds} = 2.0 \text{ V}$ . The maximum external

transconductance is 440 mS/mm and the saturated current (at  $V_{gs} = 0$ ) is 36 mA.

$S$ -parameter measurements (from 2 to 40 GHz) were carried out on  $100\text{ }\mu\text{m} \times 0.1\text{ }\mu\text{m}$  pseudomorphic devices embedded in a coplanar transmission line printed directly on the wafer surface. The advantage of testing devices on wafer (e.g. using a Cascade Microtech wafer probe system) is that it speeds the gathering of statistical data (by eliminating the need for dicing chips and wire bonding). On-wafer probing also improves the accuracy of device modeling because complex fixture and wire bond de-embedding is eliminated.

Fig. 4 shows the maximum available gain and maximum stable gain ( $MAG/MSG$ ) as derived from  $S$ -parameter measurements taken from 2 to 40 GHz on an HP 8510B automatic network analyzer. The  $MSG$  is typically 13.7 dB at 18 GHz and the  $MAG$  is 7.4 dB at 40 GHz. The device  $f_T$ , as determined by extrapolating the "measured"  $H_{21}$  (including all parasitics) versus frequency to  $H_{21} = 0$ , yields a cutoff frequency of 95 GHz (see Fig. 5).

#### IV. NOISE FIGURE

The noise performance of several  $100\text{ }\mu\text{m} \times 0.1\text{ }\mu\text{m}$  PHEMT's was measured in a precision waveguide-to-microstrip test system [9] at the National Radio Astronomy Observatory. A detailed description of the test system and comparative test results on HEMT's from various suppliers, including GE and Fujitsu, are given in [9].

The room-temperature device noise figure at 43 GHz was measured to be 1.32 dB (minimum noise temperature  $T_{\min} = 103 \pm 8\text{ K}$ ) with 6.7 dB of associated gain, while at a physical temperature of 17 K the noise figure dropped to 0.36 dB ( $T_{\min} = 25 \pm 1\text{ K}$ ) with 6.9 dB of associated gain. The noise figure of an infinite cascade of identical devices, assuming optimal interstage matching, is 1.62 dB ( $T_{\text{cascade}} = 131 \pm 10\text{ K}$ ) at room temperature, and the cascaded noise figure is 0.44 dB ( $T_{\text{cascade}} = 31 \pm 1\text{ K}$ ) at 17 K physical temperature. Realistic assumptions for matching circuit and transition losses (of about 0.7 dB) yield a projected multistage amplifier noise figure of about 2.3 dB at 43 GHz employing the PHEMT's reported here.

#### V. PHEMT DESIGN ISSUES

A design consideration in achieving ultra-low-noise device performance is the trade-off between gate capacitance and transconductance. High doping levels and narrow gate-to-channel spacings not only increase transconductance but also increase gate-to-source capacitance. Low-noise device designs are guided by the empirical Fukui [11] relationship given by

$$F_{\min} = 1 + K_1 f C_{gs} \sqrt{(R_g + R_s)/g_m} \quad (1)$$

where  $F_{\min}$  is the minimum noise figure,  $f$  is the frequency of operation,  $C_{gs}$  is the equivalent gate/source capacitance,  $g_m$  is the intrinsic transconductance,  $R_g$  is the equivalent gate resistance,  $R_s$  is the equivalent source resistance, and  $K_1$  is an empirical factor related to mate-

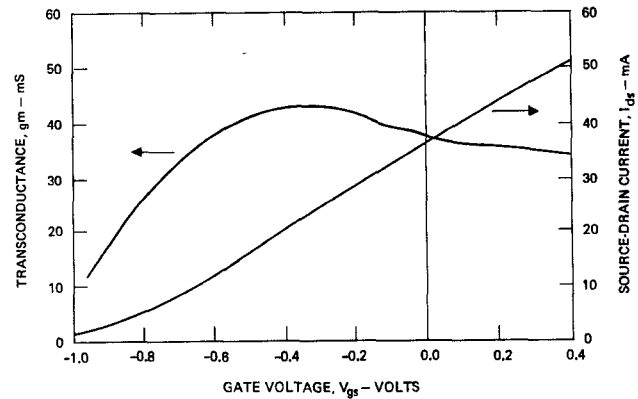


Fig. 3. dc device characteristics: drain current versus gate voltage and external transconductance versus gate voltage.

rial quality and device type ( $K_1$  is lower for HEMT's than for MESFET's).

Trading lower transconductance,  $g_m$ , for reduced gate capacitance is seen as beneficial to the noise figure so long as the parasitic fringing component of  $C_{gs}$  and the parasitic pad capacitance remain small compared to the depletion layer component of  $C_{gs}$ . For example, in [6], a  $0.08\text{-}\mu\text{m}$ -gate-length pseudomorphic HEMT is reported to have high transconductance ( $g_m = 740\text{--}920\text{ mS/mm}$ ) and also correspondingly high gate capacitance ( $C_{gs} = 1.6\text{ pF/mm}$ ). The pseudomorphic HEMT's reported here have  $g_m = 440\text{--}500\text{ mS/mm}$  but with gate capacitance of  $C_{gs} = 0.70\text{ pF/mm}$  (as determined by  $S$ -parameter measurements and optimum noise matching). The ratio  $C_{gs}/\sqrt{g_m}$ , which appears in the minimum noise figure, equation (1), is smaller for these PHEMT's ( $1.22\text{ to }1.30 \times 10^{-12}\text{ F}/\sqrt{\text{S}\cdot\text{mm}}$ ) than for the  $0.08\text{ }\mu\text{m}$  PHEMT's ( $1.67\text{ to }1.86 \times 10^{-12}\text{ F}/\sqrt{\text{S}\cdot\text{mm}}$ ) [6]. Lowering  $g_m$  does reduce both device maximum available and associated gain. A "rule of thumb" for practical device design is to establish the minimum  $g_m$  necessary to achieve an associated gain of 6–10 dB at the frequency of interest and then minimize the noise figure by reducing  $C_{gs}$  as much as possible.

#### VI. NOISE TEMPERATURE (NOISE FIGURE) COMPARISON

It is useful to establish a figure of merit for low-noise devices such that comparisons can be easily made between devices tested at different frequencies. Since noise temperature (noise figure) varies with input match and losses, drain current, bias voltage, physical temperature, and frequency, a fixed set of conditions must be selected to yield a meaningful comparison. For the proposed figure of merit, we assume that optimum drain and gate bias is applied for lowest noise and that the optimum match is applied to the device input. All pure circuit losses external to the device are subtracted out. Room temperature (293 K) is chosen as the reference temperature. Under this set of conditions, the device noise temperature  $T_n$  is equal to its minimum noise temperature,  $T_{\min}$ , which is equal to  $T_0(F_{\min} - 1)$ , where  $T_0$  is the standard noise temperature 290 K and  $F_{\min}$  is the minimum device noise figure—lin-

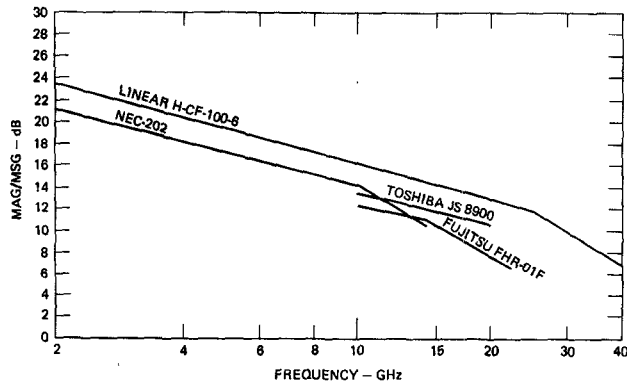


Fig. 4. PHEMT maximum available gain/maximum stable gain versus frequency. Commercial HEMT device data taken from data sheets [1]–[4].

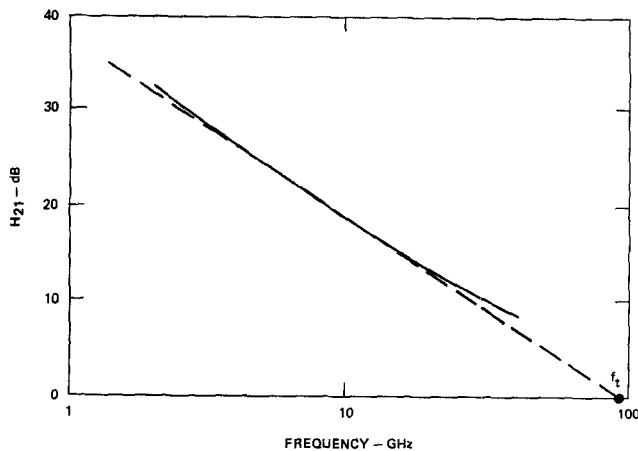


Fig. 5. Projected cutoff frequency  $f_c$  projected from  $H_{21}$  measurements (from 2 to 40 GHz).

ear not in dB. Theoretically,  $T_{\min}$  is predicted to be linearly related to frequency [10]. The linear frequency dependence of  $F_{\min}$  is also evident from empirical formulas by Fukui [11], Podell [12], and Weinreb [13]. The linear behavior of  $T_{\min}$  and  $F_{\min}$  holds true for microwave frequencies, where the device  $1/f$  noise can be neglected (usually above 1 to 2 GHz in most III–V FET devices). We define a term  $T_f = T_{\min}/f_{\text{test}}$  as the noise temperature figure of merit for the device under optimum match and bias conditions. Since larger noise temperatures (noise figures) are more accurately measured than low ones, the noise temperature at the maximum test frequency is used to calculate  $T_f$ . Table I gives the figure of merit  $T_f$  for several commercial and research GaAs MESFET's, HEMT's, and PHEMT's.

Fig. 6 shows a comparison of device noise figure (in dB) versus frequency for the devices listed in Table I. The noise temperature figure of merit  $T_f$  for the one tenth micrometer PHEMT discussed here is believed to be the lowest for any reported GaAs-based transistor.

Very low noise figures have recently been reported for lattice matched and pseudomorphic AlInAs/GaInAs/InP HEMT's (0.8 dB at 60 GHz [15], [16] and 1.2 dB at 58 GHz [17]). However, this new material system is presently

more difficult to grow by MBE and is less mature with regard to processing and reliability [18].

## VII. NOISE FIGURE SENSITIVITY COMPARISON

An important factor in practical transistor amplifier design is the device sensitivity to noise match. For wide-band amplifiers this sensitivity is critical because it limits the ability to achieve the lowest noise over large bandwidths. The noise temperature  $T_n$  of a two-port driven by a generator of impedance  $Z_g$  is

$$T_n = T_{\min} + \frac{(NT_0)}{R_g R_{\text{opt}}} |Z_g - Z_{\text{opt}}|^2 \quad (2)$$

where  $T_{\min}$  is the minimum noise temperature,  $N$  is the noise parameter,  $T_0$  is the standard temperature  $\approx 290$  K,  $Z_{\text{opt}}$  is the generator impedance yielding minimum noise, and  $R_g$  and  $R_{\text{opt}}$  are the real parts of  $Z_g$  and  $Z_{\text{opt}}$  respectively. The noise parameter  $N$  determines how rapidly the noise temperature increases as  $Z_g$  diverges from  $Z_{\text{opt}}$ . Low- $N$ -value devices are prized because they are less sensitive to variation in  $Z_g$  and thus are more easily matched over broad bandwidths.

The noise figure  $F$  (linear—not dB) can be similarly represented by

$$F = F_{\min} + \frac{g_n}{R_g} |Z_g - Z_{\text{opt}}|^2 \quad (3)$$

where  $F_{\min}$  is the minimum noise under optimum generator match conditions and  $g_n$  is the noise conductance. The noise parameter  $N$  and the noise conductance  $g_n$  are related by  $N = g_n R_{\text{opt}}$ . The term  $R_n$ , defined as the noise resistance, is also employed to describe device noise match sensitivity and is known to be [13]

$$R_n = \frac{N}{R_{\text{opt}}} |Z_{\text{opt}}|^2. \quad (4)$$

$N$  is a linear function of frequency so that its value must be associated with a given test (or reference) frequency [10]. Table II gives the  $N$  value of several HEMT's and PHEMT's and defines a noise parameter figure of merit  $N_f$  (i.e., the  $N$  value divided by the test frequency) for device comparison.

As discussed by Cappy [19], the noise sensitivity to mismatch of HEMT's appears to be lower than that of MESFET's. This improvement has been experimentally demonstrated for HEMT's by Pospieszalski *et al.* [20]. Table II indicates that PHEMT's exhibit a noise sensitivity advantage when compared to conventional HEMT's. The noise factor figure of merit  $N_f$  reported here is the lowest of any known GaAs transistor. Low-noise amplifiers employing PHEMT's are expected to produce better noise performance over broad bandwidths.

TABLE I  
NOISE TEMPERATURE FIGURE OF MERIT  $T_f$  FOR VARIOUS GaAs-BASED DEVICES (AT ROOM TEMPERATURE)

Supplier	Device	Model No.	$T_f = T_{\min}/f_{\text{test}}$	$f_{\text{test}}$	Reference
NEC	MESFET	NE-045	9.58 (K/GHz)	12 GHz	[1]
NEC	HEMT	NE-202	8.33 (K/GHz)	30 GHz	[1]
NEC	HEMT	NE-201	5.66 (K/GHz)	30 GHz	[1]
Fujitsu	HEMT	FHR 01X	6.45 (K/GHz)	20 GHz	[2]
Mitsubishi	HEMT	MGF4405A	7.16 (K/GHz)	18 GHz	[3]
Toshiba	HEMT	JS8901-AS	5.61 (K/GHz)	26 GHz	[4]
GE	PHEMT	----	2.68 (K/GHz)	59.3 GHz	[6]
GE	HEMT	----	2.48 (K/GHz)	60 GHz	[14]
GE	HEMT	----	2.79 (K/GHz)	43 GHz	[9]
Linear (this work)	PHEMT	H-CF-100-6	2.39 (K/GHz)	43 GHz	[9]

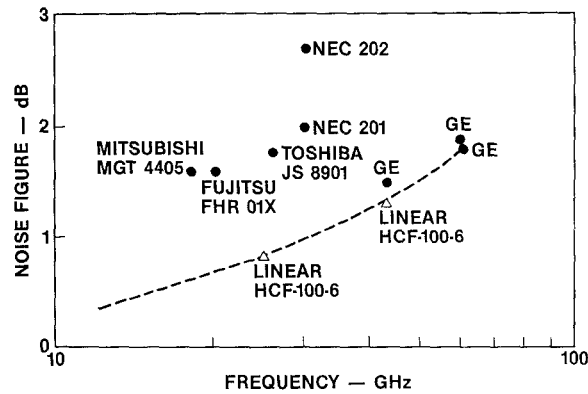


Fig. 6. Device noise figure comparison for HEMT's and PHEMT's on GaAs.

TABLE II  
NOISE PARAMETER FIGURE OF MERIT,  $N_f$ , FOR VARIOUS GaAs-BASED DEVICES (AT ROOM TEMPERATURE)

Supplier	Device	Model No.	$N$	$f_{\text{test}}$	$N_f = N/f_{\text{test}}$	Reference
NEC	HEMT	NE-202	0.47	30 GHz	$15.6 \times 10^{-3} (1/\text{GHz})$	[1]
NEC	HEMT	NE-201	0.71	30 GHz	$23.6 \times 10^{-3} (1/\text{GHz})$	[1]
Fujitsu	HEMT	FHROIX	0.19	18 GHz	$10.5 \times 10^{-3} (1/\text{GHz})$	[2]
Mitsubishi	HEMT	MGF4405A	*		*	[3]
Toshiba	HEMT	JS8901AS	0.13	18 GHz	$7.0 \times 10^{-3} (1/\text{GHz})$	[4]
GE	HEMT	----	0.39	43 GHz	$9.1 \times 10^{-3} (1/\text{GHz})$	[9]
Linear (this work)	PHEMT	H-CF-100-6	0.13	43 GHz	$3.0 \times 10^{-3} (1/\text{GHz})$	[9]

\*Measured data do not satisfy the basic noise inequality for two-ports:  $N > T_{\min}/4T_0$  [10].

### VIII. DEVICE ENHANCEMENTS

Several design and process trade-offs are possible that will enhance the performance of short-gate PHEMT's. For example, a "mushroom" shaped gate [14] will lower the equivalent resistance of the one tenth micrometer gate by a factor of 8–10 over the current design. The gain of the PHEMT can be significantly raised by implementing an "offset recess," [7] which reduces gate-to-drain feedback capacitance. Incorporation of both the mushroom gate and the offset recess into the PHEMT design will yield devices with noise figures of less than 2 dB and gains of over 10 dB at 100 GHz. These performance levels will have a significant effect on future systems since LNA's can be placed in front of mixers to enhance receiver performance.

### IX. CONCLUSIONS

State-of-the-art low-noise pseudomorphic HEMT's with gate lengths of one tenth micrometer have been produced. The devices exhibit 1.32 dB noise figure ( $T=103$  K) with 6.7 dB associated gain at 43 GHz (at room temperature). The device design has been optimized for low noise figure with good associated gain and low sensitivity to both noise match and temperature. Two figures of merit are defined, the noise temperature normalized to operating frequency ( $T_f$ ) and the noise parameter  $N$  normalized to operating frequency ( $N_f$ ). The transistors reported here have the lowest values of  $T_f$  and  $N_f$  of any reported GaAs-based device. The high  $g_m/C_{gs}$  ratio and low  $N$  value of the pseudomorphic HEMT's show significant promise to im-

pact both ultra-low-noise and ultra-broad-band systems. We anticipate that PHEMT transistors will have significant applications in satellite communication, remote sensing, electronics warfare, radar, and radio astronomy.

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#### REFERENCES

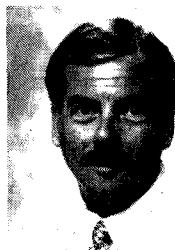
- [1] NEC Corporation, California Eastern Laboratories, Microwave Semiconductor Products, Data Sheets, 1988.
- [2] Fujitsu, Microwave Semiconductors, Data Sheets, 1987.
- [3] Mitsubishi, *GaAs Field-Effect-Transistor Data Book*, 1989.
- [4] Toshiba, Microwave Semiconductors, Data Sheet, 1987.
- [5] R. E. Lee, R. S. Beaubien, R. H. Norton, and J. W. Bacon, "Ultra-low-noise millimeter-wave pseudomorphic HEMT's" in *IEEE MTT-S Int. Microwave Symp. Dig.* June 1989, pp. 975-978.
- [6] P. C. Chao *et al.*, "DC and microwave characteristics of sub-0.1- $\mu$ m gate-length planar-doped pseudomorphic HEMT's," *IEEE Trans. Electron Devices*, vol. 36, pp. 461-472, Mar. 1989.
- [7] L. F. Lester, P. M. Smith, P. Ho, P. C. Chao, R. C. Tiberio, K. H. G. Duh and E. D. Wolf, "0.15  $\mu$ m Gate-length Double Recess Pseudomorphic HEMT with  $F_{max}$  of 350 GHz," *IEEE IEDM Technical Digest*, pp. 172-175, December 1988.
- [8] R. S. Beaubien and R. E. Lee, "Sub-micron E-beam lithography for GaAs integrated circuits," presented at IEEE Workshop on Micrometer and Submicrometer Lithography, Hyannis, MA, 1984.
- [9] S. Weinreb, R. Harris, and M. Rothman, "Millimeter-wave noise parameters of high performance HEMT's at 300 K and 17 K," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1989, pp. 813-816.
- [10] M. W. Pospieszalski, "A new approach to modeling of noise parameters of FET's and MODFET's and their frequency and temperature dependence," National Radio Astronomy Observatory, Electronics Division Rep. #279, July 1988.
- [11] H. Fukui, "Design of microwave GaAs MESFET's for broad-band low-noise amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 463-470, July 1979.
- [12] A. Podell, "A functional GaAs FET noise model," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 511-517, May 1981.
- [13] S. Weinreb, "Low-noise cooled GASFET amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 1041-1047, Oct. 1980.
- [14] K. H. G. Duh, *et al.*, "Millimeter-wave low-noise HEMT amplifiers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 1988, pp. 923-930.
- [15] U. K. Mishra *et al.*, "Noise performance of sub-micron AlInAs-GaInAs HEMT's," presented at IEEE Device Research Conference, Boulder, CO, May 1988.
- [16] U. K. Mishra, A. S. Brown, and S. E. Rosenbaum, "D. C. and R. F. performance of 0.1  $\mu$ m gate length Al<sub>0.48</sub>In<sub>0.52</sub>As-Ga<sub>0.38</sub>In<sub>0.62</sub>As Pseudomorphic HEMT's," in *IEEE IEDM Tech. Dig.*, Dec. 1988, pp. 180-183.
- [17] P. Ho, *et al.*, "Extremely high gain, low noise InAlAs/InGaAs HEMT's grown by molecular beam epitaxy," in *IEEE IEDM Tech. Dig.*, Dec. 1988, pp. 184-186.
- [18] P. M. Smith and A. W. Swanson, "HEMT's-low noise and power transistors for 1 to 100 GHz," *Appl. Microwaves*, vol. 1, pp. 63-72, May 1989.
- [19] A. Cappy, "Noise modeling and measurement techniques," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 1-10, Jan. 1988.
- [20] M. W. Pospieszalski *et al.*, "Noise parameters and light sensitivity of low noise high electron mobility transistors at 300 K and 12.5 K," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 218-233, 1986.



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